temperature

temp 1 (Acg 2)

Brief Description of Drawings These and other objects and advantages of the invention will be apparent upon reading the following description in conjunction with the drawings, in which: FIG. 1 is a block diagram of a circuit incorporating the present invention; FIG. 2 is a schematic representation of a

preferred embodiment of the tuned circuit of FIG. 1; FIG. 3 is the block diagram of a second alternate embodiment of the circuit of the invention; and . FIG. 4 is the schematic representation of the integrator shown in block 4 ing FIG. 3.

Description of the Preferred Embodiments:

Referring to FIG.1, the circuit breaker of the invention comprises a tuned circuit 3 connected between the poles 1 and 2 of the supply line to the device to be protected. The operation of the circuit breaker of the invention is based on the random pulses that are generated by an electric arc in a supply line. These pulses shock excite the tuned circuit 3. The signal, after amplification by amplifier 4, continues to monostable 11, then to a counter circuit 13 resetted by timer 12, finally it trips the breaker activation circuit 5 which causes the contacts of the circuit breaker 6 to open. (b) means of means The circuit of the invention avoids that the

The circuit of the invention avoids that the signals emitted by the motors with brushes or tyristor controlled light attenuators that are connected to the supply line 1, and excite the tuned circuit 3, improperly trip the circuit breaker. Brush motors emit a continuos gapless signal and thyristors produce constant phase narrow pulses, the inventor AUC 1 includes means to prevent these interferences from tripping the circuit breaker, according to what follow 1: The time constant of the monostable circuit 11 is adjusted to be close to the duration of one cycle of the

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adjusted to be close to the duration of one cycle of the supply line frequency. A steady pulse input signal coupled from the A. C. supply line through tuned circuit 3 and amplifier 4 for mantains the monostable output at a fixed logic level; more precisely, said steady pulse retriggers the monostable 11. An interruption of the input signal produces a pulse at the output of the monostable circuit, this pulse being counted by a counter 13 connected to the output of the monostable circuit 11.

Counter 13 is periodically reset to zero by timer 12. If the count reaches a predetermined number, 8 or 16, in less than approximately 1.5 seconds, the breaker activation circuit 5 is tripped, opening the contacts of the circuit breaker 6. If the count in the counter does not reach the predetermined number in the 1.5 second time period, timer 12 resets counter 13 to zero and the count starts over again.

The improvement is based on the fact that the electric arc, besides generating random phase pulses, also exhibits random interruptions in the flow, presumably caused by the

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